Claims 21-40 are added and submitted for favorable consideration. No new matter has been added to the specification.

Reconsideration of the application in light of the above amendments and the following remarks is respectfully requested.

Applicants submit that cited reference, U.S. Patent No. 5,886,706 (the Alcorn patent), fails to describe the claimed invention. For example, in claim 21, Alcorn fails to describe a controller module, coupled to the cache module and the address module, adapted to respond to the first pixel identifier corresponding to the first memory block by synchronizing the non-stalled transmission from the cache module of a first texel within the first memory block and the non-stalled storage of a second memory block of the plurality of memory blocks from the memory module in the cache module; said first texel corresponding to the first pixel identifier. Rather, Alcorn appears to disclose a caching system that uses a cache directory to determine whether a block of texture data is stored within the cache (column 13, lines 7-11). If the texture data is not found (miss) in the cache, the cache directory generates an *interrupt* control signal that is sent to the host computer which causes the processor to retrieve the data from the memory (column 13, lines 34-42). As this data is being retrieved from the memory, subsequent retrieval of new texture is interrupted (column 14, line 10-14). As a result, a miss in the cache memory may

cause a backup or stall in the pipeline of either the texture mapping board or the frame buffer board (column 14, lines 5-8).

With regard to independent claim 30, Alcorn fails to describe a retrieval controller, coupled to the data reference counter, adapted to respond to the first value having a value at least equal to a second value by triggering the storing of a second memory block of a second plurality of memory blocks from the memory module in the cache module; said second value representing a number of consecutive texels corresponding to a first transmit tag signal. As discussed above, in Alcorn there appears to be no risk of premature overwriting of data within the cache because Alcorn relies upon an interrupt signal whenever there is a cache miss.

With regard to independent claim 32, Alcorn fails to describe the step of responding to the first pixel identifier corresponding to the first memory block by synchronizing the non-stalled transmission from the cache module of a first texel within the first memory block from the cache module and the non-stalled storage of a second memory block of the plurality of memory blocks from the memory module in the cache module. Instead, Alcorn appears to disclose a system that relies upon an *interrupt* control signal to cause the processor to retrieve the data from the memory (column 13, lines 34-42). As this data is being retrieved from the memory, subsequent retrieval of new texture is interrupted or stalled (column 14, line 10-14). As a result, a miss in the cache memory may cause a backup or stall in the pipeline of either the texture mapping board or the frame buffer board (column 14, lines 5-8).

As to dependent claims 22-29, 31 and 33-40, Alcorn does not disclose the many distinct features of these claims. For example, there is no discussion in Alcorn of a retrieval controller (claim 25), a status module (claim 31) or a step for responding to a first value having a value at least equal to a second value by triggering the storing of a second memory block of a plurality of memory blocks from the memory module in the cache module (claim 40).

For the foregoing reasons, it is respectfully submitted that claims 21-40 are in condition for allowance. Favorable action, therefore, is solicited.

Respectfully submitted,

DONG-YING KUO; ZHOU HONG; RANDY ZHAO;
ROGER NIU; POORNACHANDRA RAO; JEREMY ALVES

By: _____

Douglas B. Luftman, Reg. No. 43,762
FENWICK & WEST LLP
Two Palo Alto Square
Palo Alto, CA 94306
Tel: (650) 858-7182
Fax: (650) 494-1417